Abstract

A constant-transconductance rail-to-rail CMOS input circuit with offset trim is provided. PMOS and NMOS differential trim stages are scaled versions of PMOS and NMOS input stages respectively. The differential trim stages are configured to adjust the offset of the differential output current with accuracy over temperature. A first current mirror circuit is configured to receive a fraction of a bias current (βI), where β is related to the input common mode voltage. A second current mirror circuit is configured to receive another fraction of the bias current ($(1-\beta)I$). The first current mirror circuit is configured to provide current βI to the PMOS input stage, and a scaled-down version of current βI to the PMOS differential trim stage. The second current mirror circuit is configured to provide current $(1-\beta)I$ to the NMOS input stage, and a scaled-down version of current $(1-\beta)I$ to the differential PMOS trim stage.